REMARKS

The undersigned and the Examiner conducted a telephone interview on April 25, 2006. The Examiner's rejections presented in the Final Office Action and potential amendments to the claims were discussed. No conclusion was reached.

Applicants propose amending independent claims 1, 10, and 17, as indicated above. Applicants also propose cancelling claims 3, 12, and 19. Applicants respectfully submit that the proposed amendments place the present application in better condition for appeal or allowance and therefore respectfully request that the Examiner enter the proposed amendments. Pursuant to the proposed amendments, claims 1-2, 4-11, 13-18, and 20-22 are pending in the present application.

In the Office Action, claims 1-22 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. Claims 3, 12, and 19 have been canceled, rendering the Examiner's rejections of these claims moot. The Examiner's remaining rejections are respectfully traversed.

First, the Examiner alleges that independent claims 1, 10, and 17 are unclear because it is not clear which clause is modified by the phrase "based on a constraint length." Pursuant to the proposed amendments, Applicants respectfully submit that independent claims 1, 10, and 17 clearly set forth that the known symbols are inserted with a periodicity determined by a constraint length of an encoder.

Second, the Examiner alleges that the phrase "produce a channel coded data stream such that the number of connections between trellis nodes in a trellis are reduced" is unclear. The Examiner further alleges that this phrase should be interpreted as "produce a channel coded data

stream such that the number of connections between trellis nodes in a trellis may be ignored by a decoder at a receiving end" because a trellis is just a state machine expanded in time such that all the connections in the state diagram still exist in the trellis. Applicants respectfully disagree and note that trellis diagrams may be formed based on the state diagram associated with an encoder and any information regarding known symbols. The information regarding known symbols may be used to reduce the number of connections in the trellis diagram. See Patent Application, page 9, ll. 8-34. For example, the number of connections in the trellis corresponding to a conventional (K=3, l=2) convolutional encoder shown in Figure 2 may be reduced by inserting a zero periodically at the first position, as shown in Figure 3, or periodically at the second position, as shown in Figure 4.

For at least the aforementioned reasons, Applicants respectfully request that the Examiner's rejections of claims 1-22 under 35 U.S.C. § 112, second paragraph, be withdrawn.

In the Office Action, claims 1-5 and 10-22 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Simanapalli (U.S. Patent No. 6,081,921). Claims 8-9 and 15-16 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over Simanapalli in view of Kato, et al (U.S. Patent No. 5,436,918). Claims 3, 12, and 19 have been canceled, rendering the Examiner's rejections of these claims moot. The Examiner's remaining rejections are respectfully traversed.

Pursuant to the proposed amendments, independent claims 1, 10, and 17 set forth, among other things, inserting known symbols into a digital input data sequence to form an expanded digital input data sequence. The known symbols are inserted with a periodicity determined by a constraint length of an encoder. By inserting known symbols into the digital input data sequence with a periodicity determined by a constraint length of an encoder to form the expanded digital

input data sequence, the present invention may reduce the computational complexity of the channel coding system, may reduce the required memory storages, and may reduce the bit error rate. See Patent Application, page 7, ll. 16-25.

Simanapalli describes a convolutional encoder 22 that includes a bit insertion controller 28 that may interleave zero bits with input frame bits in an alternating manner. See Simanapalli, col. 3, ll. 3-18 and Figure 2. Applicants further note that Simanpalli has defined a constraint length N of the convolutional encoder 22 in a manner consistent with the definition set forth in the present application and presented one conventional example in which the constraint length appears to be six. See Simanapalli, Figure 1 and related discussion. However, simply inserting zero bits in an alternating manner, as described in Simanapalli, is not equivalent to inserting bits into a digital data sequence with a periodicity determined by a constraint length of an encoder. Accordingly, Applicants respectfully submit that Simanapalli is completely silent with regard to inserting bits into a digital data sequence with a periodicity determined by a constraint length of an encoder.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Simanapalli and request that the Examiner's rejections of claims 1-5 and 10-22 under 35 §U.S.C. 102(b) be withdrawn.

Applicants further submit that the present invention is not obvious over the prior art of record. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. As discussed above, Simanapalli does not describe or suggest inserting bits into a digital data sequence with a periodicity determined by a constraint length of an encoder. The Examiner relies upon Kato to describe reducing a number of connections between trellis nodes in a trellis by inserting fixed bits in a bit

stream. The fixed bits may be inserted near the central portion of encoding information bit data. In the case of inserting a plurality of bits, the bits may be inserted concentratedly or distributively. See Kato, col. 4, ll. 7-16 and Figures 5A-B. However, Kato is also completely silent with regard to a constraint length. Accordingly, Kato does not describe or suggest inserting bits into a digital data sequence with a periodicity determined by a constraint length of an encoder.

The cited references also fail provide any suggestion or motivation to modify the prior art to arrive at Applicants claimed invention. To the contrary, both of the cited references teach away from the Examiner's proposed modification of the prior art. Simanapalli appears to teach away from inserting bits into a digital data sequence with a periodicity determined by a constraint length of an encoder. In particular, Simanapalli describes interleaving zero bits with input frame bits in an alternating manner, *e.g.*, inserting a zero bit after every input bit. However, the convolutional encoder described in Simanapalli appears to have a constraint length of six. See Simanapalli, Figure 1 and related discussion. Kato also teaches away from the present invention. In particular, Kato teaches that fixed bits are inserted in a data stream to reduce a residual bit error ratio for the *same* line bit error ratio, whereas the present invention teaches periodically inserting known symbols to *reduce* the line bit error ratio. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not obvious over Simanapalli in view of Kato and request that the Examiner's rejections of claims 8-9 and 15-16 under 35 U.S.C. §103(a) be withdrawn.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

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